Claims

What is claimed is:

1. A circuit configurable for indicating a voltage level of an input signal applied to the circuit, the circuit comprising:

at least one transistor, the at least one transistor including a first terminal connected to a first voltage supply, a second terminal configured for receiving the input signal, and a third terminal operatively coupled to an output of the circuit; and

a passive load connected between the third terminal of the at least one transistor and a second voltage supply;

wherein the circuit is configured to generate an output signal at the output of the circuit, wherein the output signal being at a first value indicates that the input signal is substantially at a first voltage level, and wherein the output signal being at a second value indicates that the input signal is substantially at a second voltage level.

2. The circuit of claim 1, wherein the first voltage supply is a positive voltage supply and the second voltage supply is a negative voltage supply with respect to the first voltage supply.

3. The circuit of claim1, further comprising a buffer circuit connected in series between the third terminal of the at least one transistor and the output of the circuit.

4. The circuit of claim1, further comprising an inverter operatively connected in series between the third terminal of the at least one transistor and the output of the circuit.

5. The circuit of claim 1, wherein the passive load comprises a resistor including a first terminal connected to the third terminal of the at least one transistor and a second terminal connected to the second voltage supply.

6. The circuit of claim 1, wherein the at least one transistor comprises a p-type metal-oxide-semiconductor (PMOS) device, and wherein the first, second and third terminals of the at least one transistor comprises source, gate and drain terminals, respectively, of the PMOS device.

7. The circuit of claim 1, wherein the at least one transistor comprises an n-type metal-oxide-semiconductor (NMOS) device, and wherein the first, second and third terminals of the at least one transistor comprises source, gate and drain terminals, respectively, of the NMOS device.

8. The circuit of claim 1, wherein the first voltage level is about 1.8 volts and the second voltage level is about 3.3 volts.

9. The circuit of claim 1, further comprising a voltage level shift circuit connected between the first voltage supply and the first terminal of the at least one transistor, the voltage level shift circuit being operative to generate a voltage drop between the first voltage supply and the first terminal of the at least one transistor.

10. The circuit of claim 9, wherein the voltage drop generated by the voltage level shift circuit is substantially greater than or equal to a difference between a maximum tolerance limit associated with the first voltage supply and a minimum tolerance limit associated with a highest expected voltage level of the input signal.

11. The circuit of claim 9, wherein the voltage level shift circuit is configurable for receiving a control signal, the voltage level shift circuit being operative to selectively vary the voltage drop in response to the control signal.

12. The circuit of claim 9, wherein the voltage level shift circuit comprises:

a second transistor, the second transistor including a first terminal connected to the first terminal of the at least one transistor, the second transistor including second and third terminals connected to the first voltage supply of the circuit; and

a passive load connected between the first terminal of the second transistor and the second voltage supply.

13. The circuit of claim 12, wherein the voltage level shift circuit further comprises a switch including a first terminal connected to the first voltage supply, a second terminal connected to the first terminal of the second transistor, and a third terminal configured for receiving a control signal presented to the switch, the switch being operative to selectively provide an electrical connection between the first and second terminals of the switch in response to the control signal.

14. The circuit of claim 12, wherein the voltage level shift circuit further comprises a third transistor, the third transistor including first and second terminals connected to the first and second terminals, respectively, of the second transistor, and a third terminal configured for receiving the input signal, the third transistor being operative to selectively shunt the second transistor in response to the input signal.

15. An integrated circuit device including at least one circuit configurable for indicating a voltage level of an input signal applied to the circuit, the at least one circuit comprising:

at least one transistor, the at least one transistor including a first terminal connected to a first voltage supply, a second terminal configured for receiving the input signal, and a third terminal operatively coupled to an output of the circuit; and

a passive load connected between the third terminal of the at least one transistor and a second voltage supply;

wherein the circuit is configured to generate an output signal at the output of the circuit, wherein the output signal being at a first value indicates that the input signal is substantially

at a first voltage level, and wherein the output signal being at a second value indicates that the input signal is substantially at a second voltage level.

16. The device of claim 15, wherein the at least one transistor comprises one of a p-type metal-oxide-semiconductor (PMOS) transistor and an n-type metal-oxide-semiconductor (NMOS) transistor, and wherein the first, second and third terminals of the at least one transistor comprises source, gate and drain terminals, respectively, of the PMOS and NMOS transistors.

17. The device of claim 15, wherein the at least one circuit further comprises a voltage level shift circuit connected between the first voltage supply and the first terminal of the at least one transistor, the voltage level shift circuit being operative to generate a voltage drop between the first voltage supply and the first terminal of the at least one transistor.

18. The device of claim 17, wherein the voltage drop generated by the voltage level shift circuit is substantially greater than or equal to a difference between a maximum tolerance limit associated with the first voltage supply and a minimum tolerance limit associated with a highest expected voltage level of the input signal.

19. The device of claim 17, wherein the voltage level shift circuit is configurable for receiving a control signal, the voltage level shift circuit being operative to selectively vary the voltage drop in response to the control signal.

20. The device of claim 17, wherein the voltage level shift circuit comprises:

a second transistor, the second transistor including a first terminal connected to the first terminal of the at least one transistor, the second transistor including second and third terminals connected to the first voltage supply of the circuit; and

a passive load connected between the first terminal of the second transistor and the second voltage supply.

21. The circuit of claim 20, wherein the voltage level shift circuit further comprises a switch including a first terminal connected to the first voltage supply, a second terminal connected to the first terminal of the second transistor, and a third terminal configured for receiving a control signal presented to the switch, the switch being operative to selectively provide an electrical connection between the first and second terminals of the switch in response to the control signal.

22. The circuit of claim 20, wherein the voltage level shift circuit further comprises a third transistor, the third transistor including first and second terminals connected to the first and second terminals, respectively, of the second transistor, and a third terminal configured for receiving the input signal, the third transistor being operative to selectively shunt the second transistor in response to the input signal.